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Akida Pico IP Datasheet

Ultra-Low-Power Time Series-Based Neural Processing IP

1. Product Overview

Akida Pico is an ultra-low-power event-based neural processing IP optimized for always-on sensing and inference in battery-powered and energy-harvesting devices. It executes Temporal Event-based Neural Networks (TENNs) entirely in the µW power range and can operate autonomously without a host CPU, waking the host only on meaningful events.

2. Key Differentiators

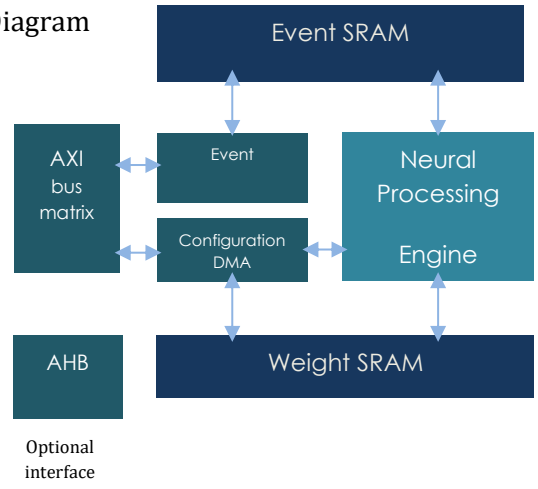
- Standalone always-on AI inference in the µW range
- Minimal buffering and ultra-low latency event-based processing
- Tiny silicon footprint enabling integration into space-constrained devices
- Purpose-built TENNs architecture for long temporal 1D sensor data (audio, IMU, vibration)

3. Architecture Overview

Akida Pico integrates a single Neural Processing Engine with on-chip memory and DMA subsystems into a self-contained accelerator. The architecture is optimized for temporal inference on time series streams rather than frame-based processing.

Figure 1. Akida Pico Block Diagram

akida pico



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3.1 Example System Integration

In typical systems, Akida Pico operates as an always-on accelerator that can be combined with an ultra-low-power MCU or directly connected to a host SoC. In an always-on, wake-up mode Pico instances are attached directly to sensor paths (PDM microphone, IMU, or other streaming sensor), to perform continuous inference, and raise a simple interrupt event to the host only when actionable conditions are detected.

4. Core Specifications

Parameter	Value
Process Technology (nominal)	22nm CMOS
Logic Gates	~160K gates
On-Chip SRAM	~74K (Event + Weight)
Clock Frequency	0 to 500 MHz (configurable)
Die Area	~0.145 mm^2 total (~0.11 mm^2 SRAM)
Compute Engine	Single Neural Processing Engine (TENNs)

5. Power Characteristics

Mode	Power	Notes
Active Inference	~50 µW avg total duty cycle	Always-on keyword spotting @ 50MHz
Leakage	~14 µW	Library and process dependent
Total Always-On	~64 µW	Duty-cycle average

6. Interfaces

Interface	Description
AXI-4	Primary system bus master interface
AHB (optional)	Lightweight host integration
SPI	Sensor data input and host communication
I2C	Sensor control via external MCU
GPIO	Interrupt / wake event output
PDM	Direct microphone connection and clock generation

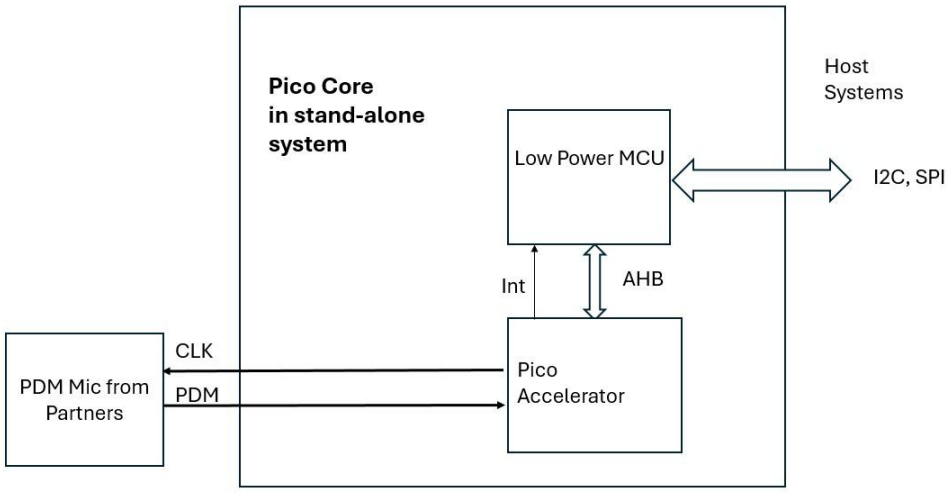
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7. Autonomous Mode

A Pico system can be configured to run autonomously, without any input or supervision from a host system. This enables the full system, except for the Pico block, to be put in a sleep state, from which it can be woken by the Pico output. Examples where this may be useful are to use Pico to detect wake-words in an audio feed, or anomalous inputs from a sensor of some kind. The diagram below shows a typical autonomous Pico configuration for audio and IMU inputs.

Figure 2. Akida Pico Configuration for Audio Inputs



The Ultra Low Power MCU integrated with Pico primarily manages comms to I2C or other serial sensors. It can also write and read data from Pico Accelerator.

2. Pico Accelerator can directly communicate with host system if MCU is not required.
3. Pico Accelerator can directly output an Interrupt on a generic Digital I/O line.
4. Pico Accelerator can output clock to PDM mic – this can be made switchable if a codec chip has to take over clock + mic after wakeup.
5. Pico directly demodulates PDM signal using internal digital filter algorithm (1-D CNN). This is also switchable.

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8. Target Applications

- Always-on keyword spotting and voice wake
- Audio preprocessing and noise suppression
- IMU-based gesture recognition and fall detection
- Medical vitals monitoring and anomaly detection
- Industrial vibration analysis and predictive maintenance

9. Software and Development Tools

Akida Pico is supported by the MetaTF development framework, enabling developers to create, train, quantize, and deploy models using TensorFlow workflow. Models are based on a unique Temporal Event-based Neural Networks (TENNs) models and can be validated using cycle-accurate simulation prior to deployment.

The MetaTF model workflow is the foundation supporting multiple AI Application Development and Deployment scenarios for users with different levels of AI Expertise and network model customization needs.

BrainChip supports a a version of MetaTF to develop TENNS models that ultimately deploy on the Akida Pico Processor. Akida Pico is based on a unique TENNs model support that does not support CNN models. This provides restricted model set enables stand-alone operation at ultra-low power levels. The TENNs model can wake-up execution on a larger NPU to execute CNN and other model classes.

Options for AI Application Development and Deployment on Akida Platform

- Native MetaTF support for TENNs Custom AI Models
- Turnkey AI Application Providers for No AI Expertise with Authorized Partners